Project Number: 766719
Start Date of Project: 2017/11/01
Duration: 45 months

Deliverable 2.2 – V1.0

Title: Demonstration of an optimised waveguide or cavity technology design with optical losses below 20 cm^{-1} for ≤ 10 µm active material operating between 2 and 10 THz

Dissemination level	Public
Submission Date	30/07/2021
Work Package	WP2
Task	T2.2
Type	Demonstrator
Version	1.0
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1. Forewords

This task is aimed at developing the simulation, fabrication and measurements to demonstrate waveguide designs with losses below 20 cm^{-1} between 2 and 10 THz. This condition is dictated by the foreseeable gain achievable with our quantum cascade laser (QCL) design at room temperature, as detailed in D5.1. Indeed, minimising the loss in any waveguide or laser cavity is key to being able to achieve net optical gain and consequently lasing with our quantum cascade design: the lower the waveguide losses then the lower the laser threshold. The project has chosen 20 meV (= 4.84 THz = 62.2 µm wavelength) for the operation of the QCL so WP2 is aiming to optimize waveguide designs at this wavelength. There are 3 tasks in the project which relate to single plasmon waveguides, double plasmon (or double metal) waveguides, and stationary plasmon waveguides. In the first year task 2.1 on single plasmon waveguides was to be completed. Tasks 2.2 on double plasmon with deliverable D2.1 for designing a WG or cavity technology with losses below 25 cm^{-1} for ≤ 10 µm of active material operating between 2 and 10 THz has already been achieved.
In this deliverable, we demonstrate the first fabricated double metal waveguides for Ge/SiGe active region material.
Device fabrication was delayed due to a series of issues at UGLA with personnel and cleanroom downtime, as already anticipated in D1.5. Furthermore, the UGLA clean room facility and device fabrication tools, have been working in a reduced way due to lockdown restrictions for the Covid 19 pandemics, allowing only a maximum of 20% utility of any laboratory since March 2020. Therefore, a measurement campaign of the waveguide losses has only recently started.

2. Simulations

The commercial photonics design package Lumerical has been used to simulate the losses in both single and double plasmon waveguides. The full details of the modelling were provided in D2.1 and only results appropriate for the double metal waveguides for D2.2 will be presented. The simulations are for $Si_{0.1}Ge_{0.9}$ but the actual material used is more appropriate for the strain symmetrised active regions in the project with an average Ge content of 95%, as required by the QCL design.
Figure 1 shows a double metal waveguide with Ag metal top and bottom.

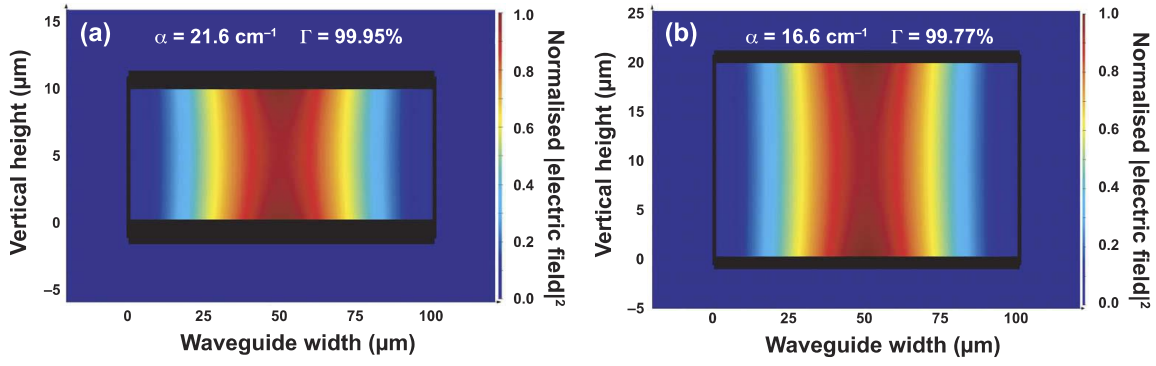

Fig. 1: (a) Lumerical simulations showing the normalised squared electric field at 4.79 THz (62.6 µm) in a 100 µm wide $Si_{0.1}Ge_{0.9}$ ridge of 10 µm depth with 50 nm n-Ge top and bottom contacts and a 400 nm Ag metal top and bottom double metal waveguide [2]. (b) The normalised squared electric field at 4.79 THz (62.6 µm) in a 100 µm wide $Si_{0.1}Ge_{0.9}$ ridge of 20 µm depth with 10 nm n-Ge top and bottom contacts and a 400 nm Ag metal top and bottom double metal waveguide.

Panel (a) shows a structure similar to that used in part 3 for the experimental waveguide devices, but using the theoretically best metal Ag (issues related with CMOS compatibility will be discussed in the following). The obtained losses of 21.6 cm^{-1} for a modal overlap of 99.95% are comparable to experimental results in the III-V system [1]. Panel (b) shows the losses can be reduced further if the active regions is increased to 20 µm thickness and the n-Ge contacts are reduced in thickness. Figure 2 shows that a reduction in the operating frequency of QCL featuring the same total thickness of 10 µm thick results in lower losses at RT= 300 K. Figure 3 shows that by reducing the temperature below room temperature also results in both the waveguide loss and the threshold gain reducing for the same 10 µm thick double metal waveguide. Therefore the project has designs that can meet the requirement of deliverable D2.2 with losses below 20 cm^{-1} for ≤ 10 µm of active material operating between 2 and 10 THz.

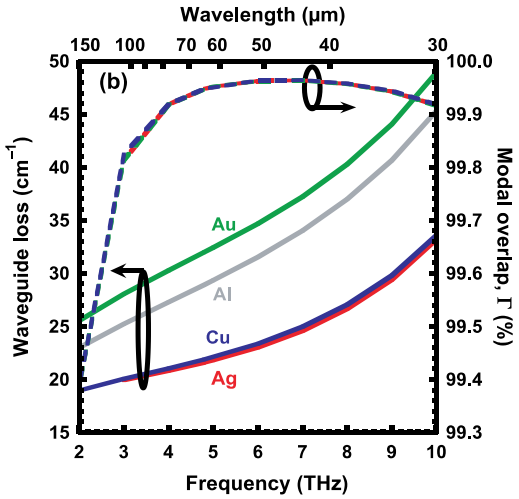

Fig. 2: The waveguide losses (left axis) and modal overlaps (right axis) at 300 K for double metal waveguides on a 100 µm wide ridge with 50 nm n-Ge top and bottom contact layers for 10 µm thick active region thicknesses for four different metals as a function of frequency.

At present the modelling has looked at conservative thicknesses for doped Ohmic contact layers with minimum values of 50 nm for the n-Ge. The top contact layer could be reduced to decrease waveguide losses further but it is quite difficult to reduce the thickness of the bottom contact layer in both of the single and double plasmon waveguide designs. For the single plasmon waveguide it becomes more difficult to etch and stop on a thin doped region and also as the thickness of the doping decreases, whilst the waveguide losses reduce the series resistance of the contact increases which will add heating to the device. For the double plasmon waveguide, the substrate has to be etched away and it should be easier to achieve a thin bottom n-Ge contact layer.
It is interesting to notice that the expected performances of Ag-based metal WGs do not practically differ from those expected using Cu. In view of the integration of the proposed device in to a "real world" Si-CMOS technology platform this observation is of paramount importance, since Cu is now widely used as metal layer in advance CMOS fabrication. Along this line, is also important to notice that IHP has recently expanded its clean-room, with the addition of a Cu-metal layer module capabilities (see https://www.ihp-microelectronics.com/news/detail/more-space-for-top-international-research).

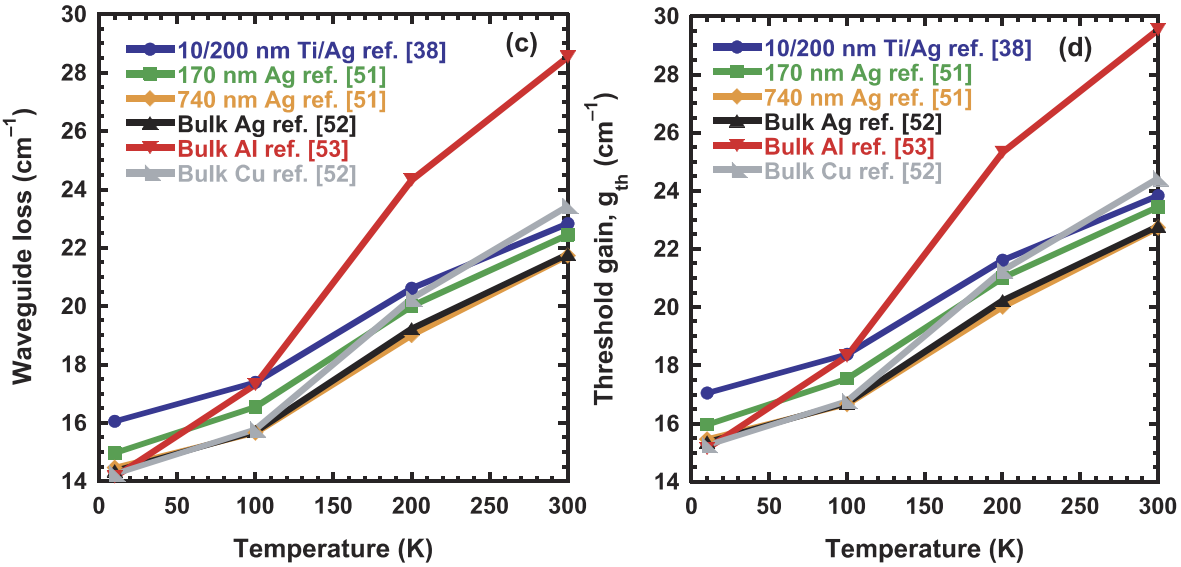

Fig. 3: The waveguide losses (left) and gain threshold (right) as a function of temperature for double metal waveguides with 10 µm $Si_{0.1}Ge_{0.9}$ active region, 50 nm n-Ge top and bottom contact layers and 400 nm of metal at 4.79 THz (62.6 µm).

3. Waveguide Design and Fabrication

A significant amount of process was required to deliver double metal waveguides with the final singulated devices having ~8.5 µm $Si_{0.05}Ge_{0.95}$ active material with 50 nm n-Ge contact layers and Ti/Au contacts shown in Fig. 6. The different steps of the fabrication process have been tested, calibrated, and optimized using samples grown at IHP and UNIROMA3. One critical issue faced was the thermal strain accumulated during the growth of our very thick samples, due to the difference in the thermal expansion parameters of the Ge-rich active and virtual substrate layers and the underlying Si substrate. Another critical issue was the calibration of the etching process to remove the thick Si substrate and the SiGe virtual substrate up to the back n^+ contact of the active region after the wafer bonding to a handle substrate. For this reason, we finally realize the process on a $Si_{0.05}Ge_{0.95}$ sample grown on a Silicon on insulator (SOI) substrate at IHP, using the SiO_2 layer as etch stop layer. Numerous attempts were made to use Ag metals as the contact layers to reduce losses but all resulted in the waveguides delaminating from the top contact bond. The full developed process is detailed below. All stages were undertaken at UGLA except the wafer bonding of the sample to a handle substrate which was undertaken at ETH Zurich.

Step	Process Detail	Status
Stage 1– Top Side Fabrication		
1	1165: 30 minutes at 50 C + Rinse with IPA and DI water	☒
2	Buffered HF dip 10:1 mixed 1:3 with DI water for 1 min	☒
3	Ar Etch over Plassys IV: 1 min 30 sec	☒
4	Top Contacts + Bond-Pads Ni/Ge/Ni – Ti/Au = 20/20/20 –15/400 nm	☒
Stage 2– Chip Bonding		
1	1165: 30 minutes at 50 C + Rinse with IPA and DI water (to remove S1818 coated for dicing)	☒
2	PECVD 80+: SiO2 ~ 2 um - Back side of the Si handle chip (Glasgow)	☒

3	Metal Deposition for bonding - Ti/Au = 15/400 nm (Glasgow)	☒
4	Chip bonding (ETH)	☒
Stage 3–Back Side Polishing		
1	PECVD 80+: SiO2 ~ 500 nm– Back side of the IHP chip	☒
2	Total thickness = 740 um 60um pad = 650 um, 9um pad = 50 um, 3 um, 1 um, 0.5 um and 0.1 um for couple of minutes Total thickness after polishing = 35-45 um	☒
Stage 4– Back Side Fabrication		
1	Dry Etch – Si Substrate STS-ICP: Amy14 = 12-15 min (3-4 um/min)	☒
2	Dry Etch - SiO_2 RIE 80+: Standard SiO_2 Etch = 12 min 30 sec	☒
3	Dry Etch - O_2 clean RIE 80+: O_2 50 SCCM, 50 mTorr, 100W = 5 min	☒
4	Photolithography for Mesa Etch Resist: AZ2070 – Spin 4K	☒
	MA6 Exposure: 20 sec	☒
	Develop: MF319 – 2 min 30 sec	☒
	Tepla O_2 Ash: 400 W, O_2 = 50 SCCM for 1 min 30 sec	☒
5	Dry Etch (WGs etch from back Si-substrate down to NiGeNi contacts) STS-ICP: FlashRYT = 20 min (inc. 4 min over etch)	☒
6	Dry Etch - O_2 clean RIE 80+: O_2 50 SCCM, 50 mTorr, 100W = 5 min	☒
7	1165: 30 min at 50 C + Rinse with IPA and DI water	☒
8	Dry Etch - Ge VS and SiGe Buffer STS-ICP: FlashRYT = 3 min STS-ICP: FlashM10 = 8-9 min	☒
9	Ar Etch over Plassys IV: 1 min 30 sec	☒
10	Back Contacts + Bond-Pads Ni/Ge/Ni – Ti/Au = 20/20/20 –15/400 nm	☒
Stage 5–Waveguide Dicing		
1	Resist: AZ2070 – Spin 4K	☐
2	WG dicing	☐

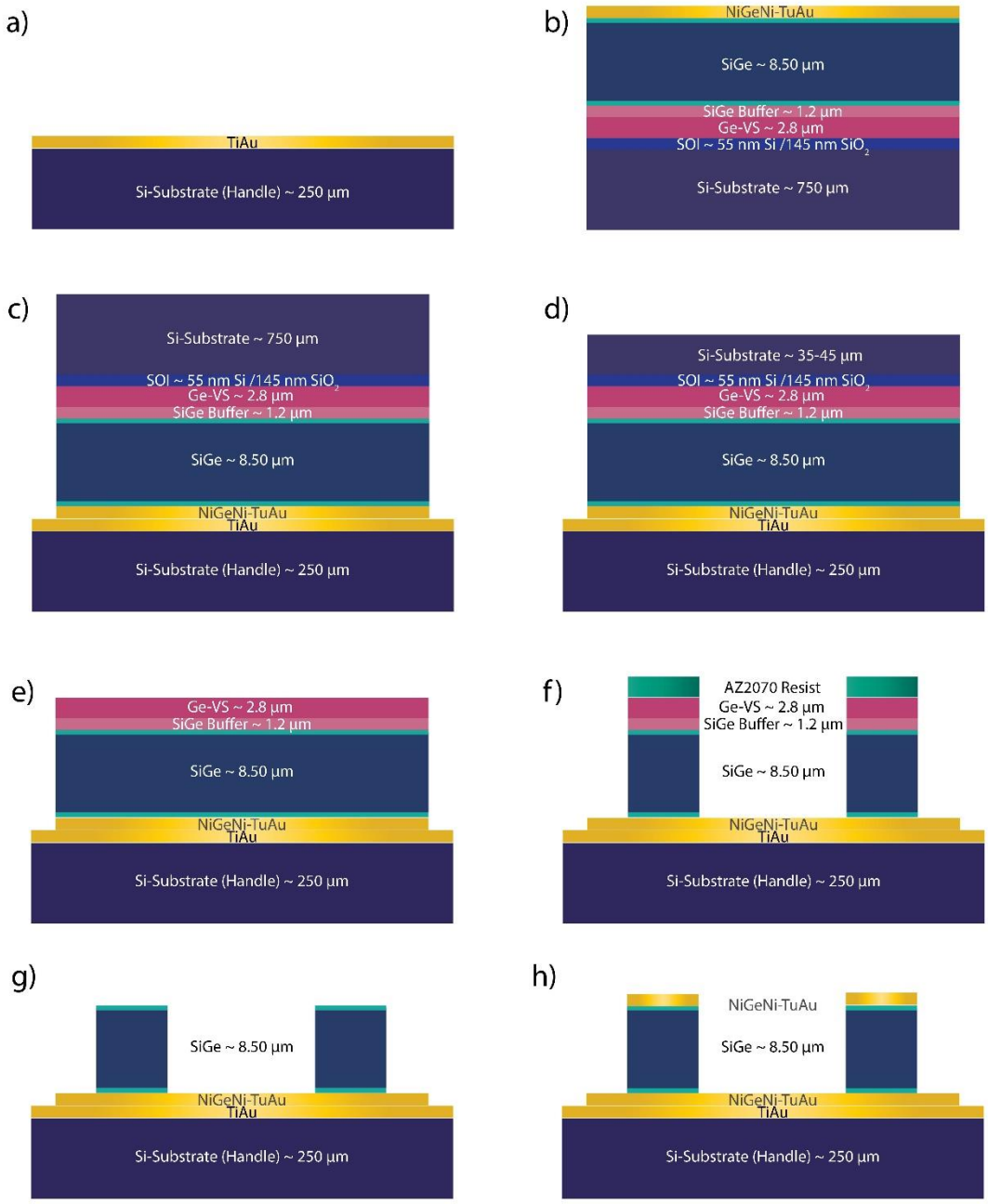

Fig. 4: Schematics of different stages of the DPWG fabrication process on a IHP-SOI chip (not scaled)
a) Si handle chip evaporated with TiAu
b) IHP-SOI chip evaporated with NiGeNi-TiAu to make ohmic contacts
c) IHP-SOI chip bonded over Si handle chip
d.) Si Substrate from IHP-SOI chip polished down to 35-45 µm
e.) Dry etch of remaining Si substrate from IHP-SOI chip using a Bosch process (SF_6/C_4F_8), where SiO_2 being used as etch stop layer, forwarded by dry etch of SiO_2 (CHF_3/Ar)
f.) Waveguides were patterned with photolithography using AZ2070 resist, over Ge-VS, forwarded by dry etch of Waveguides using a mixed process (SF_6/C_4F_8)
g.) Excess Ge-VS and SiGe Buffer etched from the Waveguides using a mixed process (SF_6/C_4F_8) to access the bottom contact
h.) NiGeNi-TiAu evaporated over the bottom contact

In Figure 4 schematics of different stages of the process are reported and in Figure 5 we show optical microscope images for a single sample at different stages of the process detailed above. In particular, we can notice the substantial roughness resulting from the grindung/polishing process used to thin the substrate down to ca. 50 µm . It was found that this mechanical thinning of the substrate was essential to reduce the heating of the samples during the final RIE removal processes, which allowed us to expose the Ge virtual substrate.

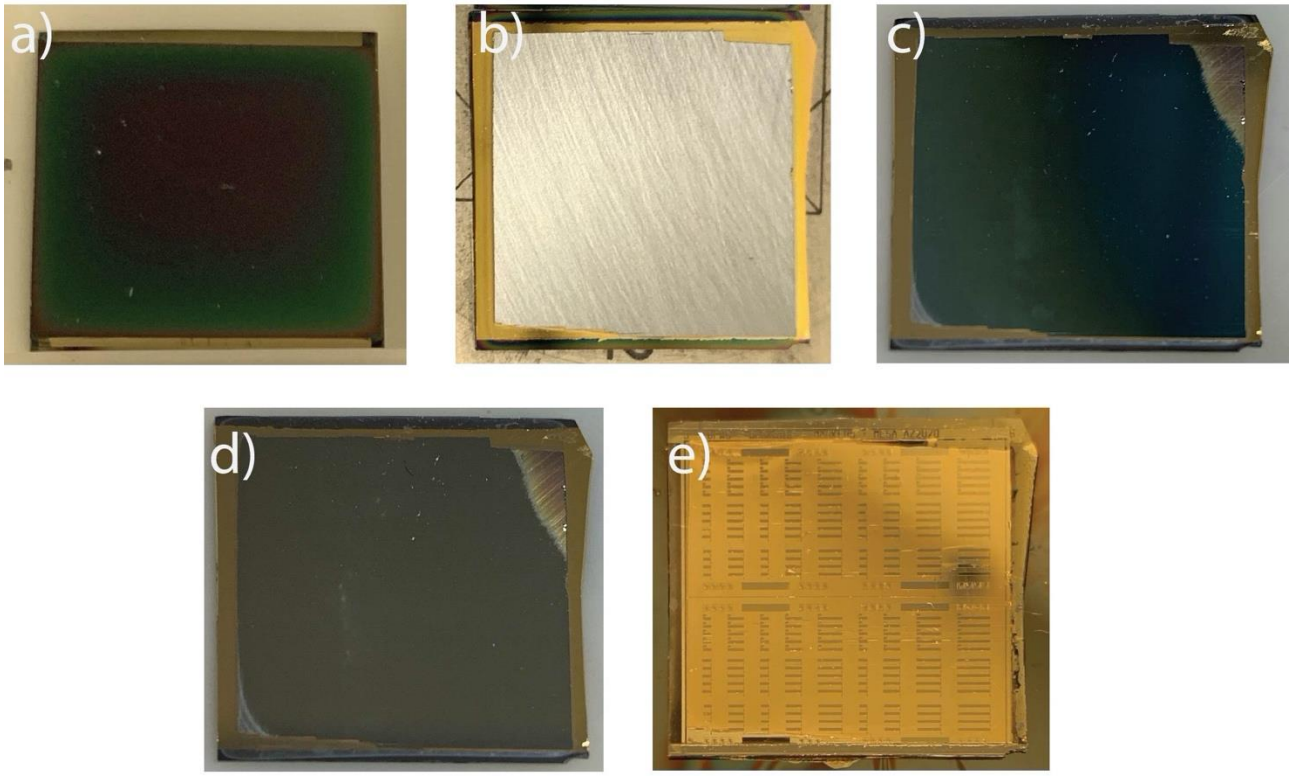

Fig. 5: a) IHP SiGe/SOI sample bonded with Si sample and deposited with SiO_2 (primarily to protect the Au from any plasma exposure or wet etching).
b) Sample polished down to ~ 50 µm.
c) Sample after RIE Bosch process removing all Si substrate and clearing any offset from the polishing (showing the SiO_2).
d) Sample after RIE SiO_2 etch (showing Ge virtual substrate).
e) Sample after 1.) etching the WGs, 2) removing Ge virtual substrate and 3) depositing Ohmic contacts.

Figure 6 shows the final devices after singulation and in the state immediately before being shipped to ETH Zurich for measurements.

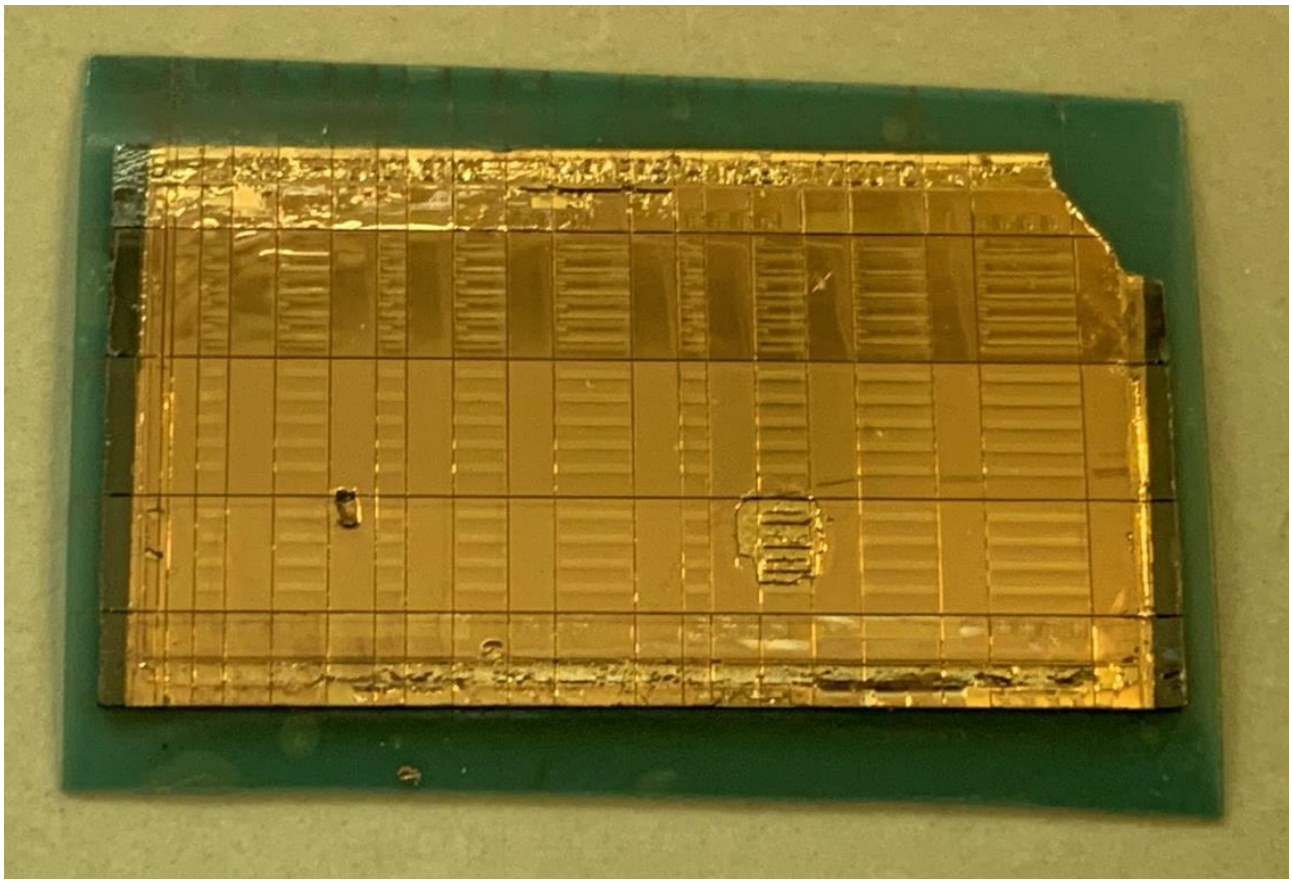

Fig. 6: A set of double metal waveguides with a range of lengths and widths on ~8.5 µm thick $Si_{0.05}Ge_{0.95}$ material with 50 nm n-Ge top and bottom contacts.

4. Experimental Measurement of Waveguide Losses

The setup for the measurements of waveguide losses is based on a commercial THz-TDS setup (TeraSmart/Menlo systems). A THz pulse is produced and detected by an ultrafast fiber oscillator and a pair of fiber coupled photoconductive antennas. The setup has already been described in details in D1.5. We report here for convenience in figure 7 the main features of the setup. This time the setup will be applied to the measurements of double metal waveguides fabricated with the process detailed in the previous paragraph of this Deliverable.

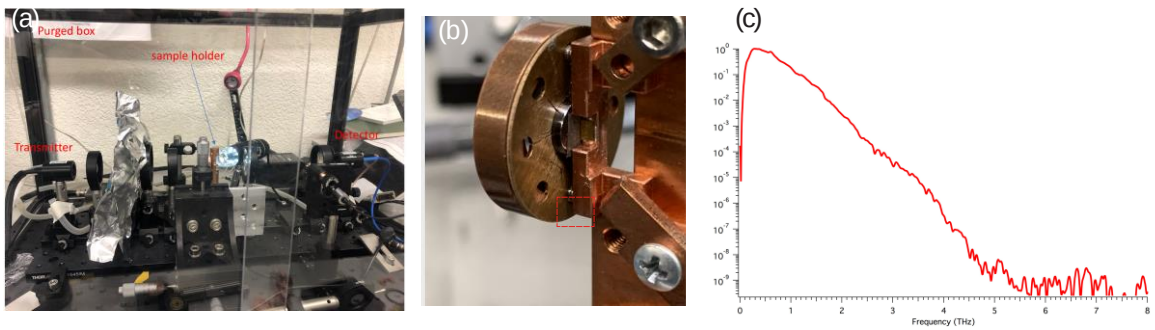

Fig.7: a) purged box with THz spectrometer. b) New support for double metal measurements with 7 mm lens and 200 x 100 um molybdenum aperture. c) typical THz transmission of the purged spectrometer without sample.

In order to optimize the setup we reduced the diameter of the coupling lens to 7 mm and we fabricated a different copper holder to have a better positioning of the lens-aperture assembly in front of the waveguide. The new support is shown in Fig. 7(b).

Two different techniques have planned in order to measure the waveguide losses in the double metal waveguide. The first one, as already described in D1.5, consists in the direct coupling via a matching lens of a free-space propagating THz pulses making use of the commercial spectrometer. The second technique relies on the on-chip production of a THz pulse via an integrated photoconductive switch, as previously demonstrated in GaAs-based THZ QCLs [3]. This technique is especially suited to the measurement of the eventual gain present in the heterostructure contained in the double metal waveguide. At the time of the writing of the present deliverable (July 2021) we could only attempt measurements on IHP samples containing a "dummy" active region and not a real gain medium. The growth process of thick QCL structure on SOI substrates has been recently developed and optimized in the UHV-CVD reactor of UNIROMA3, as described in D5.3. This will allow to fabricate double metal waveguide devices with a real gain medium in the next future.

SEM pictures of the waveguides including also integrated switches are shown in Fig.8(a-b).

Inspection of the facets of the double metal waveguides revealed some roughness due to the dry etching procedure. In order to improve the quality of the facets some FIB session were done at ETH. The resulting input and output facets of a 1 mm-long double metal waveguide are presented in Fig.8(c) (back facet) and Fig.8(d) (front facet). This is the device where the measurements have been attempted and are still currently performed at the time of the writing of this Deliverable.

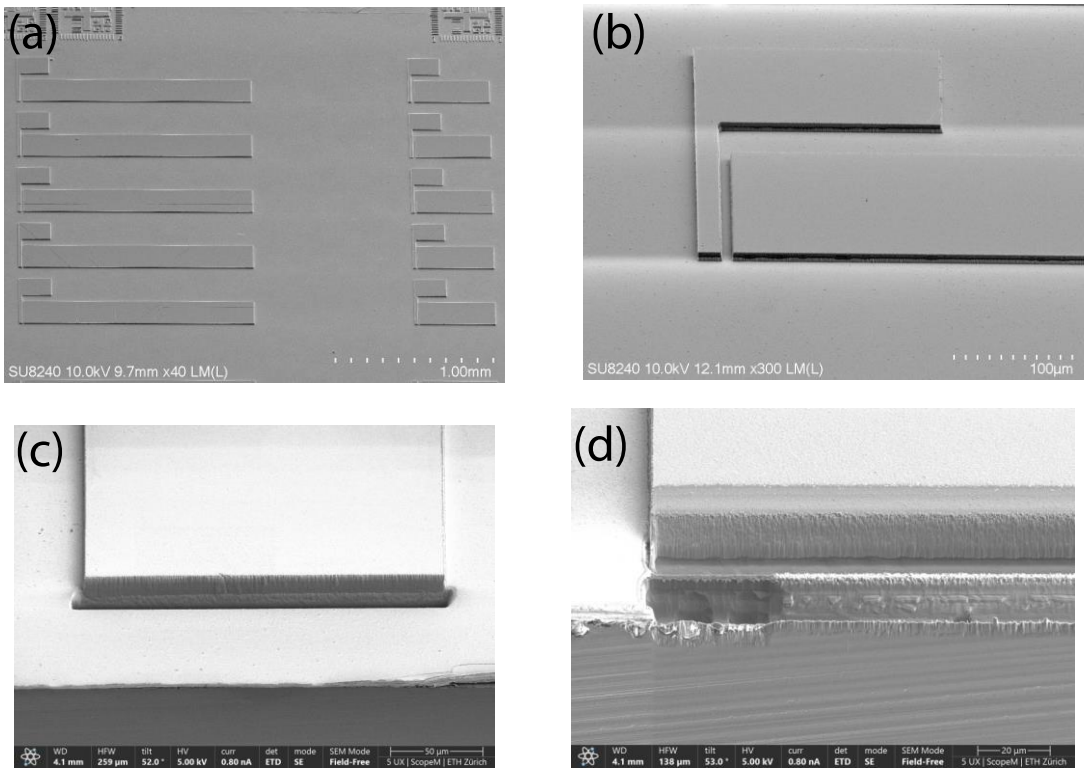

Fig.8: a) SEM picture of the processed double metal waveguides of different lengths. B) detail of a waveguide with an integrated switch for on-chip THz generation. c) back-facet rectified with FIB in order to increase the efficiency of the in-coupling and out-coupling of the THZ pulse. d) front-facet after the FIB rectification.

Unfortunately, for the moment, no signal could be detected and attributed to THz pulse propagating inside the double metal waveguide using the technique with the lens and the aperture, that is the simplest to implement experimentally as the Menlo spectrometer allows a real-time observation of the THz pulse and its Fourier transform making the pre-alignment procedure much easier.

In Fig. 9 we report some THz spectra measured with the sample presented in Fig.8(c-d) . The comparison of the empty (purged) spectrometer signal together with the one traversing the lens and the aperture is in agreement with the expectations.

The measured delay of 36.3 ps corresponds well to the one calculated with the lens diameter of 7 mm and an average refractive index of 3.35 for the Silicon (37.9 ps).

The aperture (200 x 100 um) limits the transmission at low frequencies (f<2 THz corresponding to a wavelength of 150 um in free space) and the overall signal is -20 dB lower.

In panels c) and d) we report the same signals together with the one obtained with the aperture aligned with the waveguide and the one moving the apertures lower into the substrate. In both cases we observe a residual “air pulse” still in the same time domain point but no signal at the expected delay of 13 ps (for the propagation in the SiGe waveguide with an index of 3.9). The signal has been acquired for 60 minutes in order to obtain a high signal-to-noise.

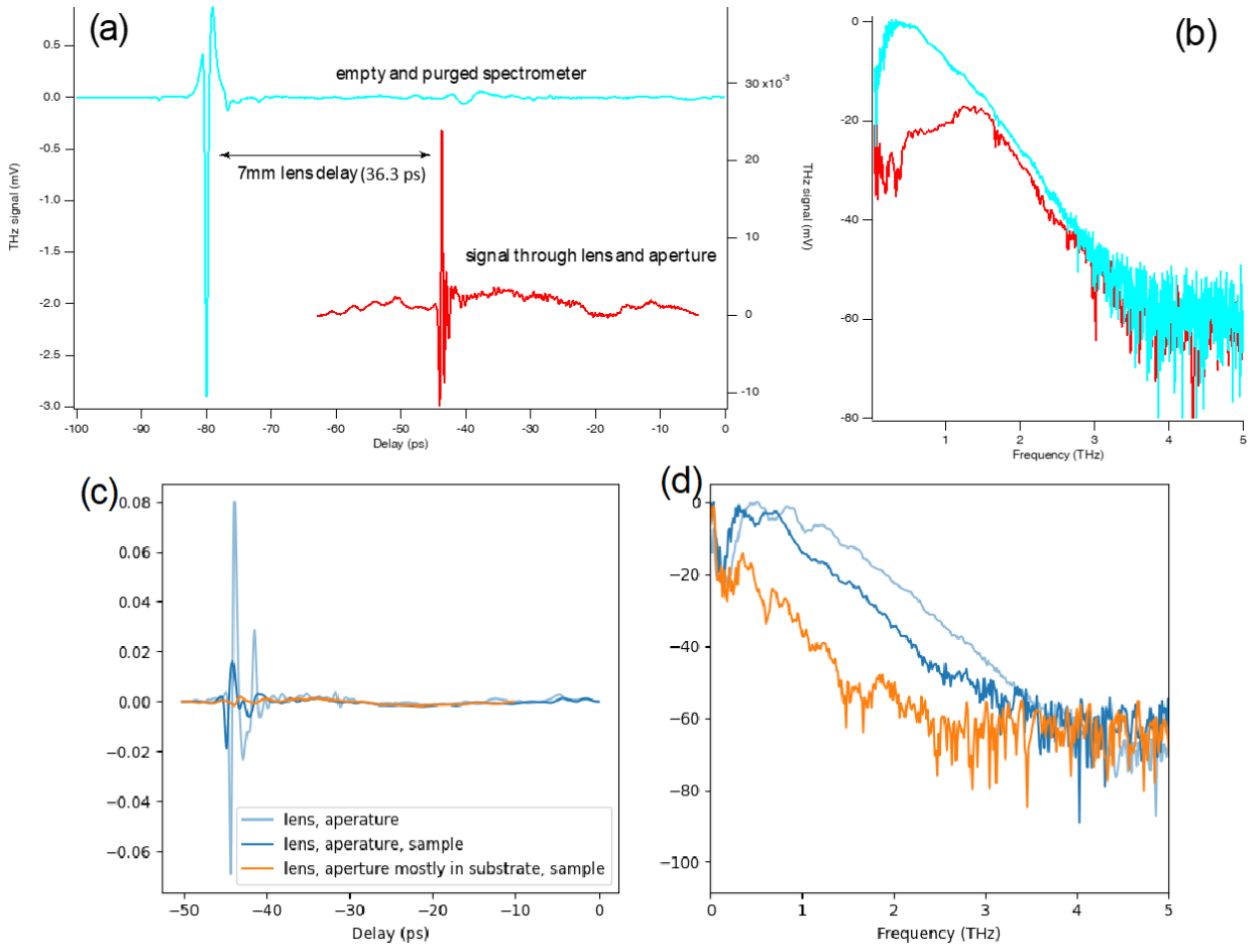

Fig.9: a) Time traces of the empty spectrometer and of the THz pulse traversing the lens plus aperture assembly. Note that the field amplitude is on the right scale for the THz pulse through the lens (red trace). (b): corresponding Fourier

transforms of the two signals presented in a). c-d) time traces and FFTs of the signals with the aperture aligned onto the waveguide and onto the substrate.

Currently the ETH group is putting in place the setup to exploit the integrated THZ switches and perform the measurement using the on-chip generation combined with far-field detection.

5. Stationary Plasmons Waveguides

Due to restricted cleanroom time from Scottish Government lockdown restrictions allowing only a maximum of 20% utility of any laboratory, the stationary plasmons were stopped due to insufficient cleanroom time to be able to deliver the devices.

6. Conclusions

The FLASH consortium was able for the first time to complete a fabrication run of double metal THz waveguides in the Si/SiGe material system. Such waveguide is the waveguide of choice for attempting a laser demonstration. A measurement campaign of the waveguide losses has been started but for the moment did not yield conclusive results.

References

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